1.   A computer system comprising:

a host processor under control of an operating system and a basic input/output system having a plurality of states, said states comprising an operating and at least one low power state;

a memory device storing the basic input/output system and the operating system for the host processor, the basic input/output systems containing code to cause the host processor to transition on request to a different state;

a first power management control register to receive the state of the host processor;

a bridge coupled to the host processor;

an I/O chip for connecting selected inputs to the bridge;

a microcontroller in the I/O chip for providing signals to the bridge from the selected inputs during operation of the computer system;

a second power management control register to store the state of the input/output chip microcontroller;

the basic input/output system for the first host processor containing code to notify the input/output chip microcontroller when the processor is to transition to a different power state.

2.   The computer of claim 1, further including:

the basic input/output system further causing the input/output chip microcontroller to transition to a like power state to that of the processor when the first processor transitions to a different power state.

3.   The computer of claim 1, further including:

the basic input/output system further causing the input/output chip

microcontroller to shut down the first processor transitions to a different power state.

4. The computer system of claim 4, wherein:

said states of the host processor include a plurality of low power states of differing levels of power consumption.

5. The computer system of claim 3, further including:

the basic input output system further causing the input/output chip microcontroller to transition to a like power state to that of the host processor when the host processor transitions to a different power state.

6. The computer system of claim 1, wherein:

the input/output chip provides run time event signals to the bridge during operation of the computer system.

7. The computer system of claim 1, wherein:

the input/output chip provides wakeup event signals to the bridge during operation of the computer system.

8. The computer system of claim 1, wherein:

the first power management register contains bits indicating the type of state of the host processor.

9. The computer system of claim 1, wherein:

the second power management register contains bits indicating the type of state of the input/output microcontroller processor.

10. The computer system of claim 1, wherein:

the first power management register contains bits indicating the type of state of the host processor; and

the second power management register contains bits indicating the type of state of the input/output microcontroller processor.

11. The computer system of claim 8, wherein:

said bits indicating the type of state of the host processor are not recognized by the bridge.

12. The computer system of claim 9, wherein:

said bits indicating the type of state of the input/output microcontroller processor are not recognized by the bridge.

13. The computer system of claim 1, wherein the host processor and its operating system are compatible with the advanced configuration and power interface specification.

14. The computer system of claim 1, further including:

a bus;

at least one peripheral device operating under control of the host processor and the operating system;

a first power management control register to store the state of the host processor;

a bridge coupled to the host processor;

an input/output chip for connecting selected inputs to the bridge;

a microcontroller in the input/output chip for providing signals to the birdge from the selected inputs during operation of the computer system;

a second power management control register to store the state of the input/output chip microcontroller;

the basic input output system for the host processor containing code to notify the peripheral device to perform a custodial function when the host processor is to transition to a different power state.

15. A computer system, comprising:

a host processor under control of an operating system and a basic input/output system and having a plurality of states, said states comprising an operating and at least one low power state;

a memory device storing the basic input/output system and the operating system for the host processor, the basic input/output system containing code to cause the host processor to transition on request to a different state;

a bus;

at least one peripheral device operating under control of the host processor and the operating system;

a first power management control register to store the state of the host processor;

a bridge coupled to the host processor;

an input/output chip for connecting selected inputs to the bridge;

a microcontroller in the input/output chip for providing signals to the bridge from the selected inputs during operation of the computer system;

a second power management control register to store the state of the input/output chip microcontroller;

the basic input output system for the host processor containing code to notify the peripheral device to perform a custodial function when the host processor is to transition to a different power state.

16. The computer system of claim 15, wherein the peripheral device responds to notification from the host processor and performs the custodial function.

17.   The computer system of claim 16, wherein the custodial function comprises storing data.

18.   The computer system of claim 16, wherein the custodial function comprises storing clock information.

19.   The computer system of claim 16, wherein the custodial function comprises unloading applications.

20.   The computer system of claim 16, wherein the custodial function comprises closing files.

21.   The computer system of claim 16, wherein the peripheral device is a wake-enabled device and wherein the custodial function comprises enabling the wake-enabled device.

22.   In a computer system having a host processor under control of an operating system and a basic input/output system, the host processor having an operating state and at least one low power state, an input/output device providing input signals to the computer system, and a microcontroller on the input/output device, a method comprising :

    detecting a command to transition the host processor to a low power state;

    notifying the microcontroller of the transition command to the host processor;

    changing the power state of the microcontroller.

23.   The method of claim 22, wherein the step of changing the power state of the microcontroller comprises changing the microcontroller to a like power state to that of the host processor.

24. The method of claim 22, wherein the step of changing the state of the microcontroller comprises shutting down the microcontroller.

25. The method of claim 22, wherein the computer system has at least one peripheral device, and further including notifying the peripheral device to perform a custodial function.

26. In a computer system having a host processor under control of an operating system and a basic input/output system, the host processor having an operating state and at least one low power state, an input/output device providing input signals to the computer system, and a microcontroller on the device, a memory device containing code causing the computer system to perform the following acts:

    detecting a command to transition the host processor to a low power state;

    notifying the microcontroller of the transition command to the host processor;

    changing the power state of the microcontroller.

27. The memory device of claim 26, wherein the memory device code causes the computer system to perform the act of changing the microcontroller to a like power state to the host processor.

28. The memory device of claim 26, wherein the memory device code causes the computer system to perform the act of shutting down the microcontroller.

29. The memory device of claim 26, wherein the computer system includes at least one peripheral device, and wherein the memory device causes the computer system to perform the act of notifying the peripheral device to perform a custodial function.